**VLSI Mini Project**

**Batch**: Monday

**Group**: 3

**Members**:

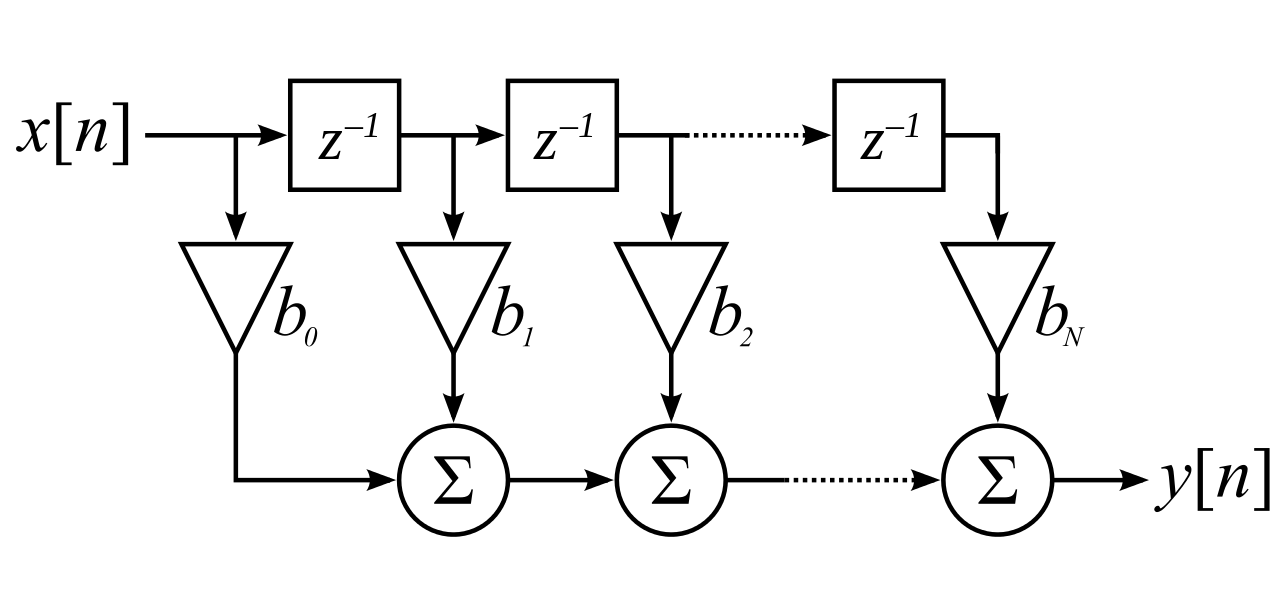
Vaibhav Krishna (16EC10064)

Divyansh Jhunjhunwala(16EC10066)

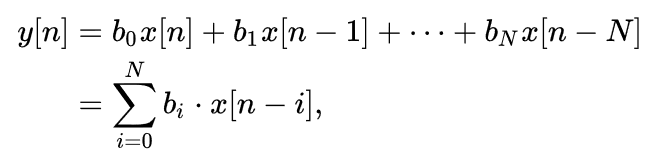
**Title**: FIR filter implementation in Verilog having signed inputs and coefficients.

**Introduction and Equations**

In signal processing, a finite impulse response (**FIR**) **filter** is a **filter** whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time.

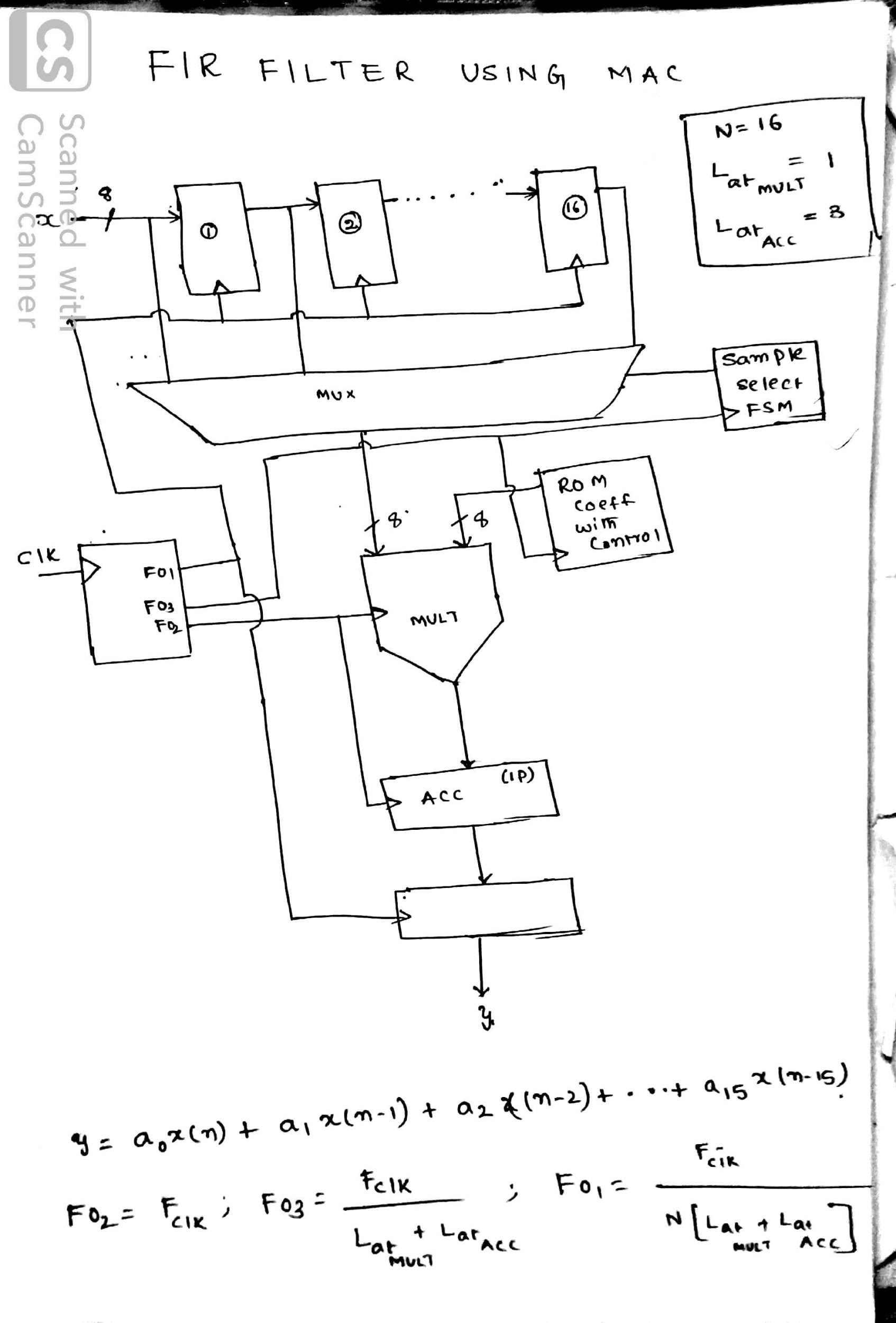


From the above image it follows that:

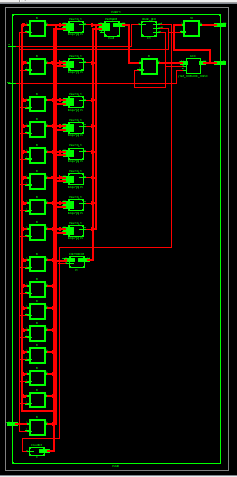


**Architecture**

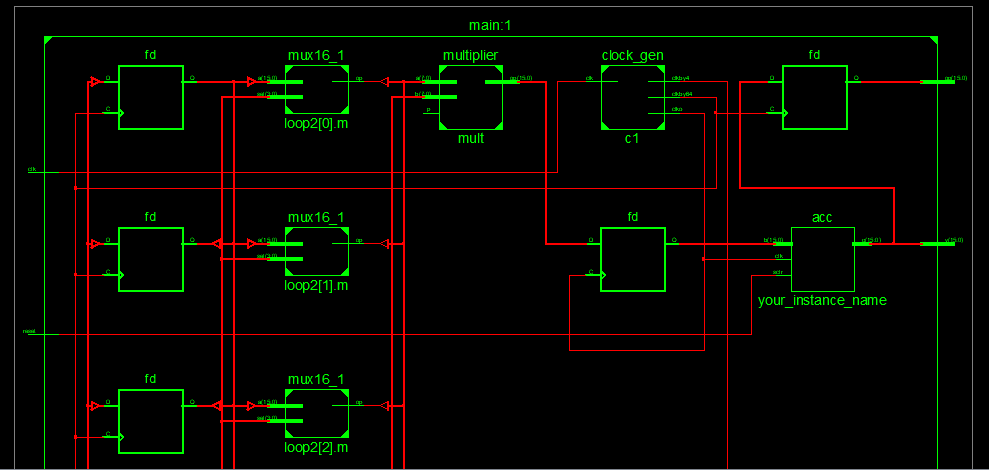
To implement the above equation in verilog we came up with the following architecture.Inputs are taken in a shift register which are the inputs to a 16x1 Mux. Then the filter coefficients are stored in a ROM, and using a counter suitable input is multiplied with the corresponding filter coefficient and then these products are added using an accumulator. After all the products are added the output is taken from the accumulator and the accumulator is reset for calculating the next filtered value.The following image outlines the above description.



**RTL Schematic**



Magnified view

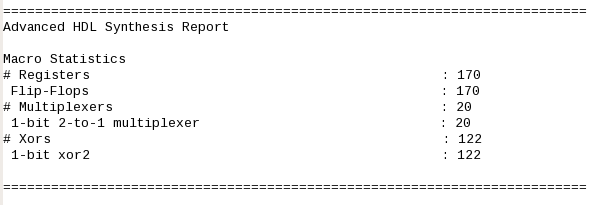
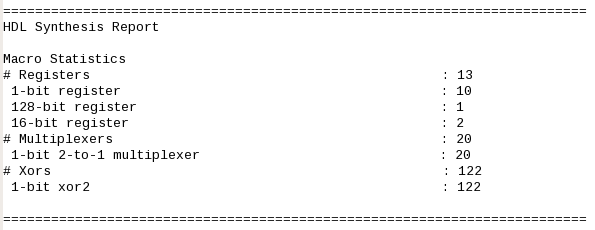
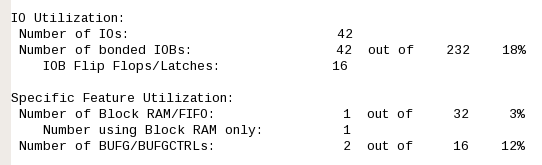
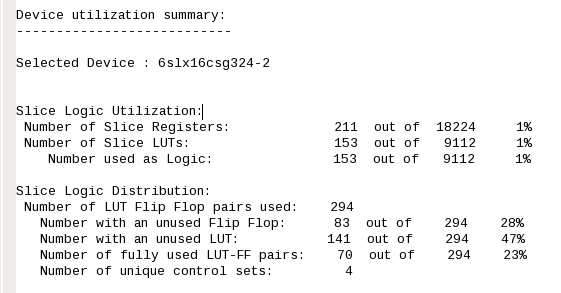


**Modules used:-**

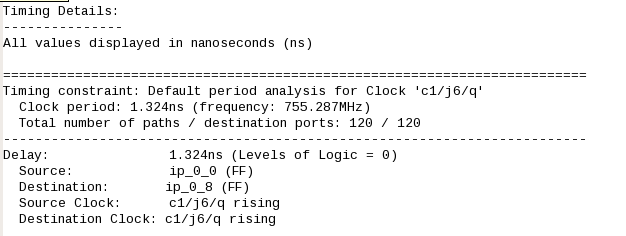
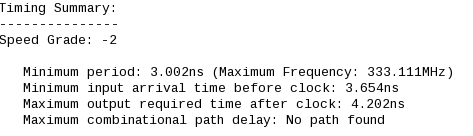
* Multiplexer 16x1
* Baugh Wooley Multiplier: Used for signed multiplication.
* Accumulator: From IPCORE
* Counter: To keep track of input from shift register
* Clock generator
* ROM : To store FIR filter coefficient. Also implemented from IPCORE

**Simulation Results:-**

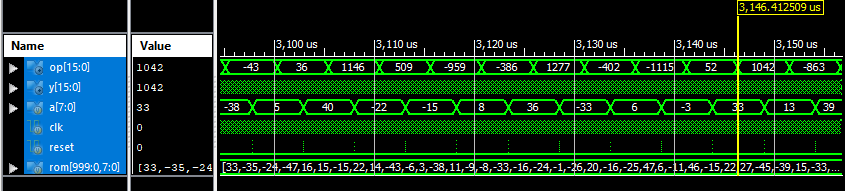
Hardware utilization:-



Timing and speed results:-



Simulation output example:



**Discussion:-**

This whole project was designed using a structural coding approach. For example to design a 16x1 Mux, 4x1 Muxes were used which were also designed using 2x1 Muxes. Even the clock generator and counter were generated using sequential logical circuits using JK Flip-Flops as the building blocks.

To reset the accumulator after taking the output, a reset input pulse was generated in the test bench as the synchronous clear(Sclr) input of the accumulator was level triggered and not edge triggered.

All the given inputs and coefficients were converted to Binary using Matlab. To initialize inputs in ROM the binary values were written in .coe format. Input is read from a text file and output is written into one for further analysis.

**Reference:**

* Zhou Yajun, Pingzheng Shi, "Distributed Arithmetic for FIR Filter implementation on FPGA", *Multimedia Technology (ICMT) 2011 International Conference*, 2011.
* A. T. Erdogan and T. Arslan "Low Power FIR Filter Implementations Based on Coefficient Ordering Algorithm". IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design, 2004 IEEE.